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Pentium® 4 Processor High-Volume Land-Grid-Array Technology: Challenges and Future Trends

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Pentium® 4 Processor High-Volume Land-Grid-Array Technology: Challenges and Future Trends

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ABSTRACT

As performance requirements for microprocessor packages and sockets increase over time, new interconnect technologies are needed to provide robust power delivery and signal integrity solutions. Traditionally, in desktop Personal Computer (PC) platforms, the state-of-the-art socketing technology for organic packages has been a surface-mounted micro-Pin-Grid-Array (mPGA) socket. However, PGA technology imposes limitations on the electrical and thermal capability and form-factor requirements of next-generation platforms. Land-Grid-Array (LGA) socket technology was developed as a means to avoid those limitations.

The feasibility of an LGA socket for the desktop PC platform was evaluated through design, prototyping, and testing. In this paper, we discuss the areas investigated during the development process, including electrical performance, mechanical loading and integrity, board routability, assembly, and reliability. The effort led to the introduction of the LGA775 socket, the industry's first high-volume LGA socket. The challenges of scaling this technology to meet the needs of future Intel® microprocessors are also discussed.

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INTRODUCTION

Since the early days of the desktop Personal Computer (PC), the microprocessor has interfaced with the system motherboard through a socket. The role of the socket is to provide electrical connectivity between the microprocessor and the motherboard, while also allowing removal and interchangeability of the microprocessor in a non-destructive fashion. Surface-mountable microprocessor packages have existed in parallel with socketable versions, but the applications for these parts have been primarily limited to market segments where a low package height is highly valued, such as mobile computers. As microprocessor speeds have continued to increase, socket requirements are becoming more challenging along two vectors. Power consumption continues to trend upward, driven by the increased leakage current of smaller silicon features, the increased dynamic current required to scale frequency, and the incorporation of multiple cores within a single package. This increased power consumption requires more interconnect contacts in order to minimize Joule heating and to meet more stringent interconnect resistance and inductance criteria. Likewise, with increased microprocessor capability, memory bandwidth is required to scale to avoid being the performance limiter in the system, leading to an increase in signal count as the number and width of bus interfaces grow. This combination of performance requirements continues to push the overall contact count higher. In today's latest PGA sockets, the pitch of the package pins and their corresponding contacts is 1.27mm, which is the minimum practical dimension from both an assembly and

reliability perspective. Therefore, significant increases in interconnect count using a PGA socket and pinned package would result in a significant increase in both package and socket size, leading to higher costs and increased real estate demands on densely-packed motherboards. Figure 1 shows an example of a PGA package and socket.

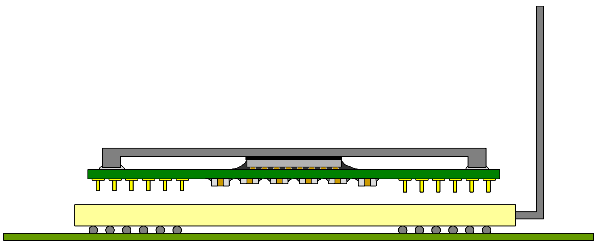

Figure 1: PGA package and socket

In response to this challenge, Intel pursued a feasibility study and development effort to enable an LGA socket that would meet the needs of desktop microprocessors in 2004 and beyond. The primary advantage of the LGA socket over PGA sockets is the ability to scale below 1.27mm pitch, allowing smaller package and socket form factors for a given contact count. Additionally, the absence of pins on the package lowers the cost of the unit. The feasibility portion of the study consisted of mechanical, electrical, and reliability testing of a microprocessor package utilizing organic package technology. Resistance of the socket contacts (bulk and interfacial) was measured under a variety of loads and environmental conditions. Once concept feasibility and fundamental boundary conditions were established, the final contact count and package/socket dimensions were refined to meet specific electrical needs, the mechanical retention hardware was designed and tested, and long-term reliability was established through environmental stressing. The final product of this development phase was a robust 775-land package/socket solution to meet the needs of Intel's 90nm Pentium® 4 microprocessor and beyond. Although LGA sockets already exist in the microprocessor industry, they are limited to the high-end server market and are predominantly paired with ceramic packages rather than the laminate packages currently on today's latest Intel microprocessors. Extending beyond this limited scope, the data collected during the development of the LGA775 socket showed that it is possible to have a reliable, affordable, high-volume LGA solution with an organic package. Figure 2 shows an example of an LGA package and socket.

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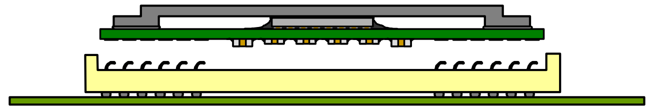


Figure 2: LGA package and socket

TECHNOLOGY DRIVERS

Mechanical, electrical, and thermal performance requirements of future Intel microprocessors are the technology drivers for microprocessor package and socket technology. In 2001, it was determined that the existing desktop socket, mPGA478, was insufficient to address the signal count and power delivery demands for upcoming processors on the roadmap. The LGA775 microprocessors and sockets in production today were the resulting solution to address these capability limitations. Determination of new form factors and sockets required a rigorous multidisciplinary study to identify and assess viable options. Customer feedback was then incorporated to close the final direction.

The input/output (I/O) signal requirements were identified as a combination of signal count and a given signal-to-ground ratio with a net performance capable of greater than 1000MT/s. Organic package technology has been utilized due to improved dielectric material properties and lower cost as compared to ceramic packages, and as such was a requirement.

Power delivery demands may generally be broken down into two parts: electrical parasitic attributes required to meet the power delivery needs of the processor, and the capability to carry the necessary current reliably. The electrical requirements are subdivided into resistance and inductance requirements. In particular, the resistance requirements are critical for carrying current in excess of 100A. The targeted improvement in the resistance path was a 50% improvement over the existing mPGA478 socket used by the 130nm and 180nm Pentium 4 microprocessors. Combined with the thermal target of socket self-heating power, and the resistance capability of options considered, the pin count demand more than doubled that of the mPGA478. To address this increase in performance, technology options covering different power delivery topologies were considered, including pin grid array, land grid array, and specialized power connectors with multiple power paths. Voltage regulation placement and the package/socket power pinout and design were additional factors considered.

While LGA sockets have been in use by high-end servers, implementations have used proprietary technologies and were not scaled to high volume. These LGA sockets also utilize double-compression LGA technology requiring gold-plated motherboard lands and ceramic

microprocessor packages. A particular implementation of LGA utilizing stamped-metal contacts was identified that offered several advantages over previous versions of LGA. The use of stamped-metal contacts allowed directly leveraging conventional high-volume socket manufacturing equipment and processes, which also made it possible to leverage PGA socket surface-mount capability.

The primary benefit of LGA technology is that it allows for pitch scaling below PGA. Since desktop systems target four-layer motherboards for optimal cost, pitch reduction and contact layout were optimized for assembly of the package, socket, and motherboard under this boundary condition. While square grid or interstitial grid pitches have been used by conventional PGA and LGA sockets, a rectangular-grid mixed pitch of 1.09mm x 1.17mm was identified as optimal from board routing and assembly standpoints. This represents a 26% contact density improvement and a 16% reduction in effective contact resistivity over PGA technology. This benefit is pronounced when viewed at the package size level: a 62% increase in pin count results in a package area increase of only 15% over the 35mm mPGA478 packages. Zero-Insertion-Force (ZIF) insertion is a benefit, as the risk of pin damage and pin true position increase with pin count for PGA options. Figure 3 shows the LGA775 and mPGA478 packages.

Figure 3: LGA775 and mPGA478 packages

The largest challenge for LGA as compared to PGA is the compressive loading requirement needed to electrically engage the contacts with the package lands. A Direct Socket Loading (DSL) concept was created to provide the sustained compressive loading between the package and socket contacts while containing this loading within the socket. Not only does the DSL provide loading sufficient for reliability interconnection, it allows for operation of a package into a socket, and allows for tool-less operation of load creation. Field serviceability and upgradeability are also improved with this option as compared to conventional server LGA implementations. These benefits mitigated the primary risks of transitioning from PGA to LGA technology.

MECHANICAL CONSIDERATIONS

Mechanical Design of LGA Socket

A new consideration for LGA sockets compared to PGA versions is the concept of loading the package in order to maintain contact with the socket contacts. In order to guarantee that this minimum load was met at all times, it was decided to incorporate DSL, a package retention and loading feature, into the socket directly. DSL is an integrated mechanism that applied a compressive mechanical load to the LGA contacts and package pads to ensure electrical continuity for the specified life of the socket. The socket consisted of a socket housing with stitched contacts, a stiffener plate, a load plate, and a load lever, as shown in Figure 4.

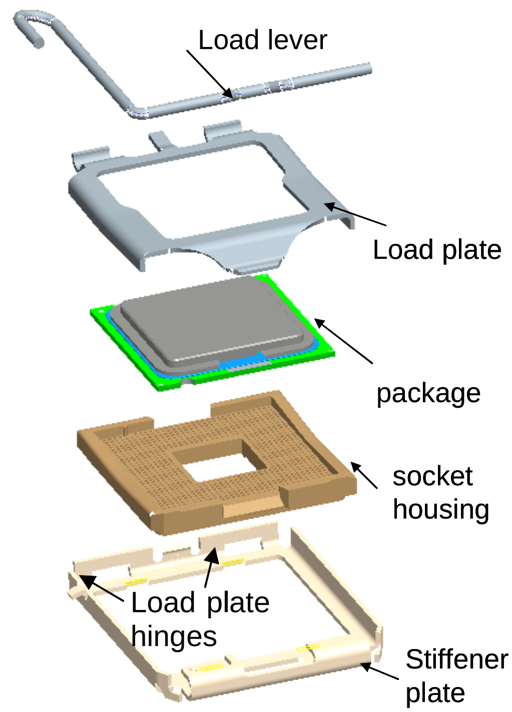


Figure 4: LGA–DSL socket exploded assembly view

Direct Socket Loading Mechanism Design

The DSL was designed to generate a minimum of 267N necessary to compress the LGA775 contacts independent of the heatsink retention solution. This load target was a product of initial feasibility studies that used a mechanical loading fixture to identify the minimum force necessary to ensure adequate contact deflection across the socket array.

In addition to the minimum load requirement, the DSL design had several other key design constraints:

1. The load plate and lever needed to remain below the top of the Integrated Heat Spreader (IHS) so that the heatsink could contact the IHS without requiring a pedestal. The IHS is a metal thermal spreader

attached to the package and the device backside to facilitate processor cooling.

2. The load plate could not contact the organic package substrate directly due to concerns about damage to the package.
3. The force to activate the load lever needed to be 40N or less to meet high-volume ergonomic standards.
4. The DSL had to meet the load requirements for package substrates with 6, 8, or 10 metal layers.

The contact activation force of 267N was generated by a two-link loading mechanism formed by the loading plate, stiffening plate, and the load lever, all of which were made from high-strength stainless steel. The load plate closed downward onto the stiffening plate about their mutual hinge points and contacted the IHS. The load lever then engaged over the top of a tab (Figure 5) on the load plate, applying a downward force on the load plate, which translated to the interface between the package and the socket contacts. Less than 9N must be applied at the load lever end to generate 267N on the package due to the mechanical advantage of 35:1 created by the combination of the load lever and load plate.

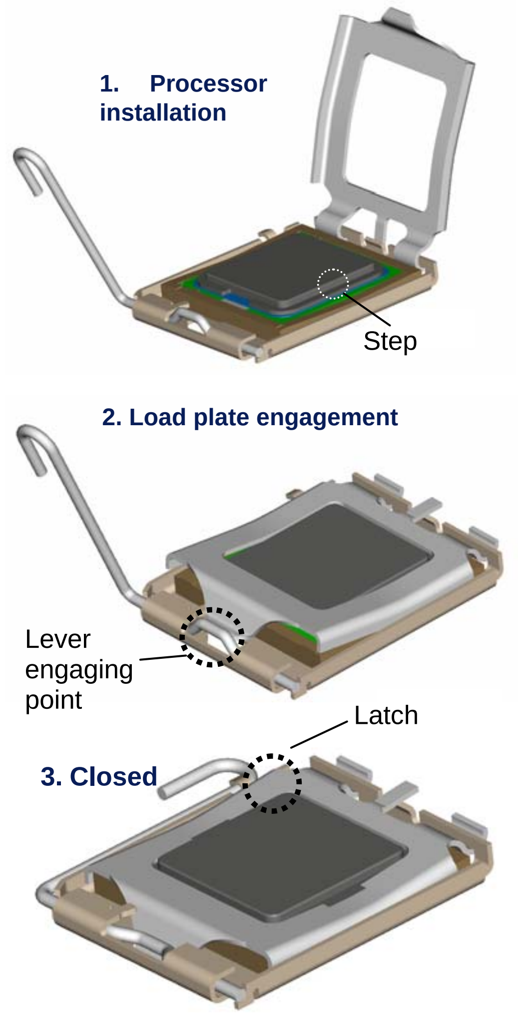


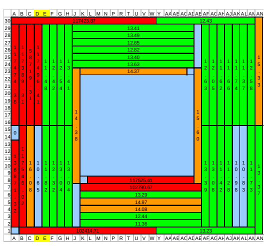
Figure 5: DSL actuation steps

The load plate had two folded edges to increase the bending stiffness and was also slightly bent upward by design to offset the bending moment during loading. The upward bend ensured that the load plate became sufficiently flat after assembly to stay below the IHS top surface when contacting the recessed step designed into the IHS, as shown in Steps 1 and 2 in Figure 5. This step provided a rigid and durable contact surface for the load plate and protected the substrate from load-induced damage.

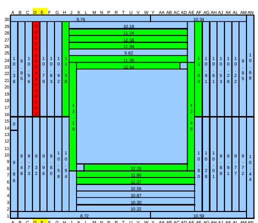
A stiffener plate under the socket prevented the bending of plastic housing during DSL loading. The stiffener plate featured a hinge interface to the load plate along one edge and a latch-type locking mechanism to hold the lever after actuation. The stiffener plate was designed to maximize bending stiffness, while minimizing the outer dimensions to avoid displacing other components on the motherboard. However, even with the optimized stiffener plate, the DSL

load generated some bending across the socket housing, creating a tensile load on the solder balls, which was detrimental to the reliability life of the socket.

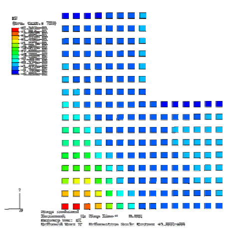
Mechanical modeling was used extensively during the design phase to simulate and calculate the DSL loads and the stresses developed in the socket and package, as well as during the socket validation phase to quantify more accurately the stresses and strains in the solder joints. The DSL load predicted by the models was ~320N, which matched the measured load to within 20%. Initial modeling also aided design modifications. For instance, the stiffener was added after identifying excessive stresses in the socket housing of the original design without the stiffener. During the validation phase, the modeling results yielded solder joint stress maps, which showed a clear correlation between the failure locations and tensile stresses in the solder joints, as shown in Figure 6. This finding helped in fixing the maximum enabling load required for socket reliability.



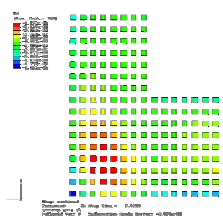
Failures after 1700 cycles of TCQ



Failures after 700 cycles of TCQ



Predicted Tensile force distribution on the BGA at 40 lbf heatsink load

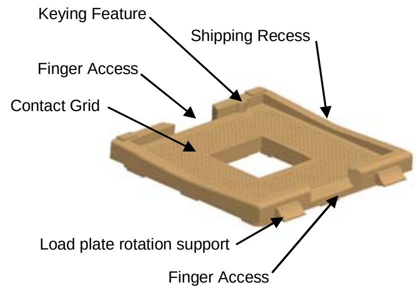


Predicted Tensile force distribution on the BGA at no heatsink load

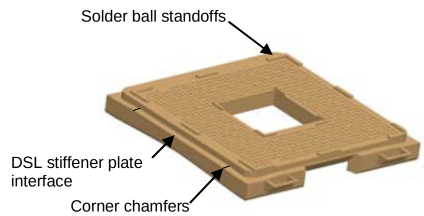
Figure 6: Comparison of the predicted vs. the experimental BGA failures in temperature cycling with the preliminary socket design. Note the failure maps and predicted tensile loading distribution correlate well qualitatively.

Socket Housing Design

The socket housing, shown in Figure 7, had many functions. It provided a support structure to hold and accurately position the contacts with a grid array of holes into which the contacts were inserted. The top face of this grid array also served as a seating plane that prevented the package from overcompressing the contacts, which could lead to damage or electrical shorting. Additionally, the raised walls around the grid array aligned the package to the socket contact array, ensuring that the socket contacts interface with the package in the proper locations.



Housing Top



Housing Bottom

Figure 7: Socket housing features

Standoffs on the housing bottom surface controlled the amount of solder ball collapse during reflow. Two cutouts on opposite sides of the housing wall were provided for finger access to allow easier package removal and installation. Recesses on the two top surfaces allowed the load plate to close without a package for shipping and board reflow. The recesses prevented the load plate from generating load while in the shipping configuration to reduce additional warpage, which would be detrimental to solder joint formation during reflow. Also, as shown in Figure 8, a taper was placed at the bottom surface of each corner to reduce the peak tension load generated by the DSL between the housing and board after reflow. This redistribution improved the reliability life of the socket.

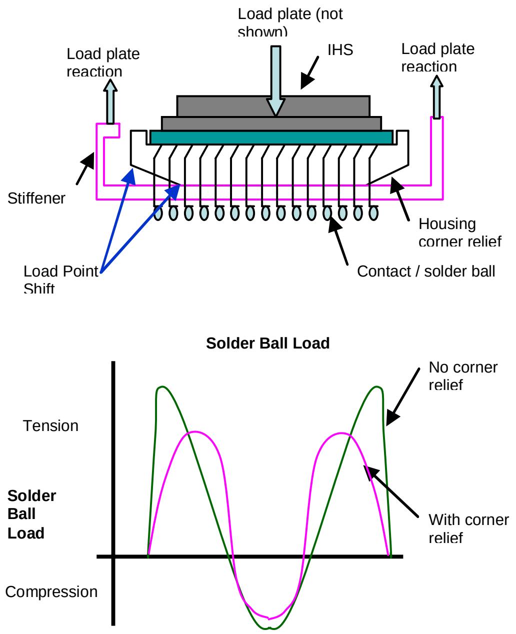


Figure 8: Corner relief feature benefits

LGA Socket Contact Design

The LGA contacts were designed to provide an adequate normal force to ensure electrical continuity at end of life. The contacts were manufactured by stamping copper alloy, which is a low-cost manufacturing option. This process yielded a minimum 0.2N normal force requirement per contact in order to meet the minimum deflection of 0.2mm necessary to meet the electrical requirements. When factoring in the warpage of the socket and package, the nominal deflection of the contacts was 0.4mm.

Socket Reliability

The reliability of the initial socket design was evaluated under various reliability stresses including temperature cycle (T/C), high-temperature bake, Highly-Accelerated Stress Test (HAST), and mechanical shock and vibration.

The failure modes observed during HAST (high electrical resistance) were due to the socket contact tip hitting the solder mask on the package rather than the metal pad. The contact tip was subsequently redesigned to keep the wipe motion near the center of the pad, and the tip was also rounded to prevent it from hitting the solder mask.

Failure analysis after temperature cycle testing showed cracks due to fatigue. Improvements were made to the socket solder ball attach processes to enhance the interface strength between the socket contact paddle and the solder ball. These process improvements helped to eliminate cracks between the contact paddle and solder ball, but introduced fatigue cracks between the solder ball and the motherboard pads. A comparative analysis of the contact design for different suppliers for compliance showed that one contact design had two 90° bends which helped to lower the strain energy transfer to the solder ball during reliability testing. This suggests that the strain energy due to compressive loading is taken up by the socket contact in this design, but directly transferred to the solder ball in the other. This finding prompted both contact redesign and optimization of the ball attach process including reflow profile, flux volume, and reflow speed, among other factors. Table 1 shows the failure rate in the socket before and after the design and process improvements when subjected to limited environmental stressing.

Table 1: Failure rate in socket before and after the design improvements

Stress	Before	After
Temperature Cycle "X" (-40ºC - 85ºC) – 1000 cycles	6/6	0/18
Bake (125°C) – 960 hrs	0/24	0/24
Mechanical Shock	8/10	0/10
Vibration	2/10	0/10

More comprehensive testing using a full suite of stresses and larger sample sizes was successfully executed with the final designs. Table 2 identifies the environmental stresses used to assess each of the 7-year and 10-year use conditions.

Table 2: Stress conditions for each use condition environment

Stress Condition	7-Year Life Expectation	10-Year Life Expectation
Temperature Cycle	1500 cycles with a mean $\Delta T = 40^oC$	2150 cycles with a mean $\Delta T = 40^oC$
Temperature/Humidity/Bias	62,000 hrs at 30^oC, 85% RH	89,000 hrs at 30^oC, 85% RH
Bake	62,000 hrs at 100^oC	89,000 hrs at 100^oC
Mechanical Shock 50 g trapezoidal profile: 170^o/sec Velocity change: 11 ms duration pulse	Total of 18 drops: 3 drops per axis ± direction	
Mechanical Vibration 3.13 g RMS, random, 5 Hz – 20 Hz .01 g2/Hz sloping up to .02 g2/Hz 20 – 500 Hz .02 g@/Hz	10 minutes/axis, 3 axes	

Socket durability testing consisted of actuating the socket 20 times, removing and replacing the package each time. Meeting electrical resistance targets, not having any visual socket irregularities, and not having any cracked solder balls under cross-section observation, were the criteria for passing the durability requirement. Earlier tested units showed intermittent failures due to the shifting of the package within the socket housing. This was caused by unbalanced loading, where the force from the load plate pushed the package against the wall along the lever side of the socket and damaged the socket by skiving the plastic in the base. To correct this, the load plate was modified to maintain the same loading location at the middle of the package throughout the actuation (Figure 9), thereby eliminating the intermittent fails.

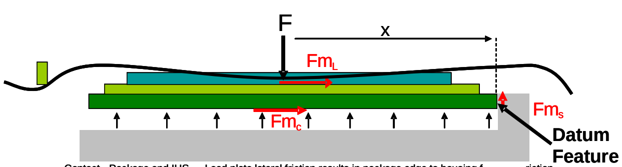


Figure 9: Load point shift to minimize package/socket friction and balance load

Integrated DSL/Heatsink Retention Mechanism

An alternate concept was developed that integrated some elements of the DSL stiffener plate with the heatsink Retention Mechanism (RM). The design goals of this concept were twofold: reduce socket bending and provide mounting points for the heatsink. Reducing socket bending would reduce the tensile loads in the corner solder balls, increasing reliability.

In this concept, shown in Figure 10, the integrated heatsink RM/socket load frame would be assembled to the LGA socket housing as well as the load plate and load lever. This assembly would then be attached to the motherboard by the socket solder balls during the reflow process. The next step would be to fasten the four corners of the load frame to the motherboard with snap or through-mounted fasteners. The processor heatsink would then be then snapped to the features in the load frame corners during final system assembly.

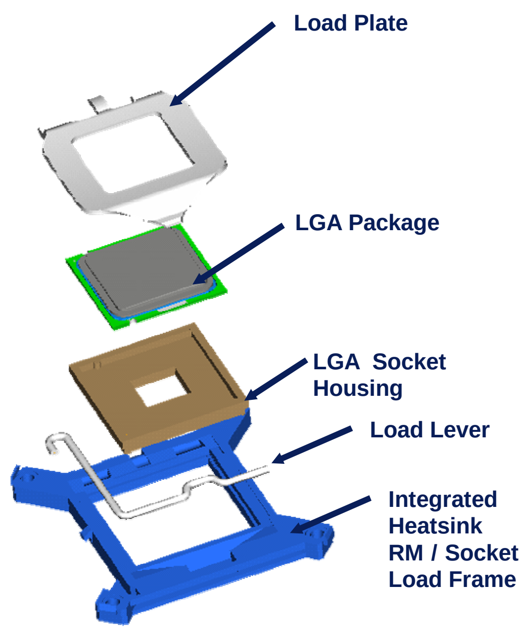


Figure 10: Exploded view of integrated DSL/heatsink retention mechanism

Although this solution improved solder joint reliability, it introduced significant technical and business implementation challenges. The technical challenge was the overall size of the load frame, which exceeded the size capability of industry pick-and-place equipment, while the fine solder ball pitch of the socket prevented manual placement, which would also be a costly assembly option. The business challenge was that computer manufacturers need to have the ability to have different heatsink interfaces for their systems. While standards do exist, custom system designs would force multiple socket and motherboard designs, which would not be cost-effective for the desktop market.

This design approach was not ultimately selected for the final socket loading mechanism as the independent socket

loading mechanism had sufficient solder ball reliability life, and the two challenges mentioned were a significant impediment to the adoption and ramp of the LGA socket design.

ELECTRICAL CONSIDERATIONS

In electrical models, the LGA socket can be represented by series inductor and resistor elements. Although both of these elements govern electrical performance, the reduction of the resistance element is a major consideration in socket development. Socket resistance is directly related to the significant issue of power dissipation. The power dissipated by the power delivery network through Joule heating is a function of the square of the current and is linearly proportional to the resistance. The current typically increases with each new technology. Because there are limits on power dissipation of the system, the resistance of the power delivery network is forced to decrease to compensate for increasing current.

Load line is a generalized expression that includes socket resistance. The load line describes the impedance of the power delivery system. The power delivery system includes elements such as the Voltage Regulator (VR), motherboard (MB in Figure 11), socket, and microprocessor. Each of these elements in the power delivery network causes a voltage drop due to its resistance contribution.

In order to meet system performance targets, the load line must decrease with each new technology generation. Figure 11 shows a comparison of the load line targets for the PGA and LGA platforms. Each element of the power delivery system was required to meet a load line target. To meet the overall target for the LGA platform, the socket load line was required to decrease from 0.43mΩ to 0.18mΩ.

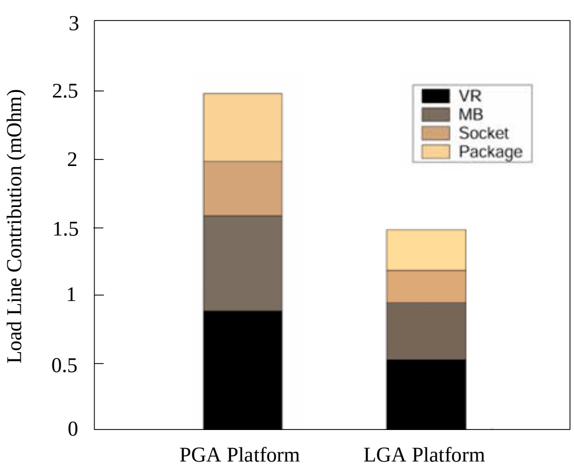


Figure 11: PGA and LGA platform load line targets

The socket load line is affected by the resistance of the socket and, most importantly, the design of the package and motherboard. The resistance of the socket contacts can easily be established through measurements. As the number of power and ground pairs in a socket increases, the number of multiple current paths also increases. The multiple current paths reduce the overall socket load line. However, the load line of a socket is strongly affected by the package and motherboard design. A socket with a high pin count could fail to meet the load line target. For example, a poorly designed pinout may cause constrictions in the current distribution, which would increase resistance. During socket development, it is critical to optimize the motherboard and package layout as well as the overall number of power and ground pairs.

Because of the design concerns related to the load line, the motherboard and package layout were taken into account during the socket design. Figure 12 illustrates the PGA and the LGA pin maps.

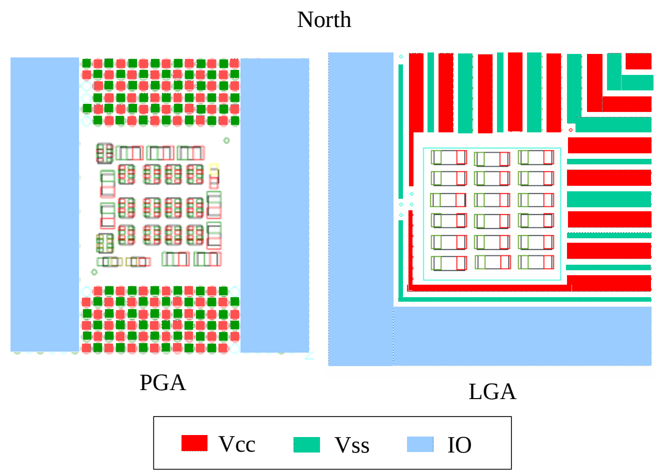


Figure 12: PGA and LGA socket pinout

The PGA pinout is shown on the left. The power and ground of the PGA design is distributed in a checkerboard pattern at the north and south sides of the socket. The VR is located at the north side of the socket. A drawback of this design is that current is not distributed equally between the north and south sides of the package because of the VR location.

Several major changes were implemented in the LGA pinout. The LGA pin map is characterized by a non-uniform pattern of power and ground pins. Power and ground pins were arranged in strips in the upper corner of the package. The VR components were placed to the north and east of the socket. This pin out and placement of the VR allowed a fairly uniform current distribution along the north and east sides of the package. Strips were used rather than a checkerboard pattern to improve current distribution near the center of the package.

The pinout of the LGA socket was designed to minimize load line. The majority of the load line reduction can be attributed to the increase in power and ground pairs. The PGA socket contained approximately 80 pairs, while the LGA socket contained close to 200 power and ground pairs. One tradeoff of the low resistance design implementation was a slight increase in the overall socket inductance.

Motherboard routing requirements were used to select the pitch of the socket contacts. A rectangular pitch of 1.09x1.17mm was utilized. The rectangular pitch allowed the board designer to escape eight rows of signals in a traditional four-layer desktop motherboard. The design rules allowed four rows of signals to escape on the surface layer and four on the base. The two internal planes were used for power delivery. A standard trace width and spacing of 127µm was used for routing. The usage of industry-standard routing rules avoided further development and cost increases to the motherboard.

Contact Resistance Assessment

One aspect of socket load line is the characterization of socket bulk and contact resistance. Socket resistance was also used by the quality and reliability team to evaluate stress-induced package failure.

A test assembly was designed to obtain contact and bulk resistance data. The assembly consisted of a socket, test package, and test board. Since the socket resistance is sensitive to the load applied by the DSL, it was critical to replicate the correct loading condition. The test assembly duplicated the product form factor and applied load.

The test setup for resistance measurements is illustrated in Figure 13. Shorts were alternately routed between the socket contacts on the test package and the test board. Once assembled, this configuration created continuous chains of socket contacts. The number of contacts per chain was limited to less than ten. This allowed for ease of fault isolation and also for chain-to-chain leakage testing. A four-wire resistance technique was utilized to remove lead resistance up to the chain. Further characterization was completed to remove the package and motherboard resistance from the measurement. The final measurement yielded an average measurement of bulk and contact resistance of the LGA socket contacts.

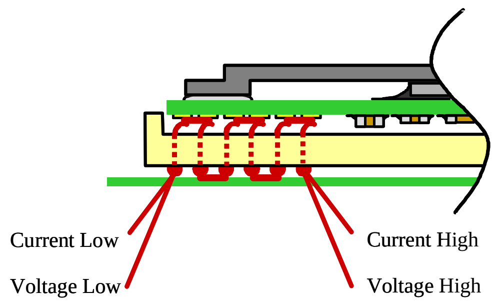


Figure 13: Socket contact resistance measurement

The assemblies were subjected to a variety of environmental stresses, as previously identified in Table 2. Socket samples from two suppliers were included in the testing.

The resistance specifications were based on the results of the environmental stress testing. Table 3 contains the final resistance specifications for the LGA775 socket. The socket resistance was specified by three values. The first value, labeled Socket Average Contact Resistance (End of Life), represents the average resistance value of a socket contact at the end-of-life condition. The second value, labeled Bulk Resistance Increase from 24°C to 100°C, limits the resistance increase due to the maximum temperature change. The two specifications are used by the electrical simulation teams to bound the worst-case socket performance. The final value, labeled Maximum Chain Contact Resistance (End of Life), was used to indicate the highest possible resistance of a single contact in a chain.

Table 3: Socket contact resistance specifications

Socket Average Contact Resistance (End of Life – room temperature)	**15.2 mOhm**
Bulk Resistance Increase from 24°C to 100°C	**3 mOhm**
Maximum Chain Contact Resistance (End of Life – room temperature)	**28 mOhm**

Maximum Temperature Assessment

As mentioned earlier, power dissipation is a linear function of resistance. Power dissipation leads to a temperature rise in the motherboard, socket, and package. The elements of the power delivery network each have temperature limits that can not be exceeded. Once a specific motherboard and package layout have been determined, it is possible to predict if the maximum socket temperature meets the 100°C limit.

The evaluation of the LGA socket utilized a DC resistance analysis of the motherboard, socket, and package, coupled with equations, to predict thermal gradients. The motherboard, socket, and package designs were divided into small sections matching the socket contact pitch. Within each section, a resistance was estimated, and a known current distribution was applied to the resistance network. The analysis yielded the current in each socket contact, and equations were developed to express the socket temperature gradient as a function of current and resistance. Once the socket contact current was known, a temperature rise was calculated. For the LGA socket, a total current of 92A yielded a maximum temperature of 93°C. The design met the temperature specifications, but it should be noted that the result is highly dependent on motherboard and package routing.

ASSEMBLY CONSIDERATIONS

As with any major technology transition, it was important to assess the impact to the customer base and then properly prepare customers in order to avoid negatively affecting their product ramps. Intel engaged with its customers on assessing assembly challenges related to the new socket more than a year prior to the product launch. The three attributes of the LGA775 socket that created the most significant challenges to Intel's customers were the mass increase to 36g (three times the mass of the PGA478 socket), the direct socket loading feature, and the exposed contacts within the socket body. Intel collaborated with leading placement, reflow, rework, and test equipment suppliers within the desktop motherboard market to establish assembly solutions for the new socket. Intel also partnered with customers to conduct experiments and assembly test board builds to identify assembly integration issues, while verifying solutions. The key recommendations based on development activities were documented in the Intel Manufacturing Advantage Services (MAS) document, training videos, and other enabling collateral.

Following the customer assessments and the development of assembly solutions for the LGA775 socket, the enabling team worked with the Intel field support teams and the socket suppliers to educate the customer base. Prior to customers beginning their initial assembly builds with the LGA775 socket, the enabling team conducted on-site plant visits to roll-out training on Surface-Mount-Technology (SMT) recommendations, the insertion/removal of the processor package into the socket, and the new test device (Intel SST) for testing the socket at in-circuit test. As product launch approached, a specific customer response focus team was formed to address customer transition questions or issues during the launch and ramp of the desktop PCs using the LGA775 socket. The team was very effective at tracking the assembly performance of the new LGA775 socket and quickly resolving any transition issues that did arise.

DISCUSSION

Given the abundance of technical challenges and lack of prior research in this area, there was significant concern whether a high-volume LGA socket combined with an organic package was a viable technology. However, the feasibility study and ensuing development program over a period of approximately four years showed that the technology was not only feasible, but also robust. The organic package was shown to be compatible with LGA technology through the use of the IHS as a mechanical load spreader; the DSL mechanism proved that LGA technology did not have to put additional burdens on customers to load the part; and high-volume, SMT, stamped-metal-contact socket technology was found to be a low-cost LGA solution.

In hindsight, the DSL mechanism has shown both advantages and disadvantages. Clearly, the ability to decouple the socket loading requirement from the thermal enabling solution is a major advantage for customers, allowing the use of less expensive materials for the heatsink retention mechanism rather than the more creep-resistant plastics that would be required to maintain the minimum socket load over the life of the system at elevated temperatures. One significant disadvantage, however, is the tensile load placed on the corner solder joints of the socket as the DSL mechanism is engaged. To avoid long-term reliability issues, this load must be

countered with an adequate compressive force from the heatsink and the motherboard. An additional disadvantage of DSL is the rather stringent package height tolerance required to keep the loading within specifications. The addition or removal of metal layers in the package, changes in die thickness or the die-package interconnect height, and changes in thermal interface material all result in overall package thickness changes that must be compensated by varying the IHS thickness.

Electrically, the ability to almost triple the number of Vcc and Vss contacts from the previous desktop socket has proven to be exceedingly useful as power delivery requirements continue to become more stringent with the introduction of microprocessors with multiple logic cores. Additionally, the more uniform current distribution across the socket due to adjacent-side power delivery provides more capability for handling the high currents associated with these new designs.

CONCLUSION

LGA775 has proven to be a significant success for Intel microprocessors. It has been shown to be a reliable mechanical design while providing substantial electrical headroom for today's and tomorrow's leading-edge microprocessors. Furthermore, it has blazed a path for future products to scale performance while minimizing package and socket growth.

Future Challenges and Trends

Extrapolating beyond the LGA775, electrical performance requirements continue to drive increases in pin count and interconnect performance. These requirements include, but are not limited to, increases in bus speed, alternative signaling technologies, feature integration, and low-voltage, high-current power delivery. Figure 14 depicts the pin count growth based on extrapolation from product trends.

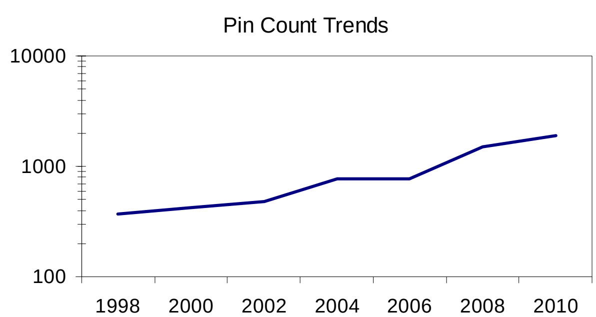


Figure 14: Pin count trends

To avoid substantial increases in package size with this increase in pin count, interconnect pitch reduction is required. Pitch reduction imposes package routing, motherboard routing, and socket design constraints that require significant integration to address. From socket design and assembly standpoints, surface-mount capability continues to be desired, imposing additional design considerations. Yield and reliability of large-pin-count and reduced-pitch components are a design challenge due to component warpage and thermal expansion differences between materials. As depicted in Figure 15, pitch reduction historically has progressed at a slower rate than pin count increases due to these constraints.

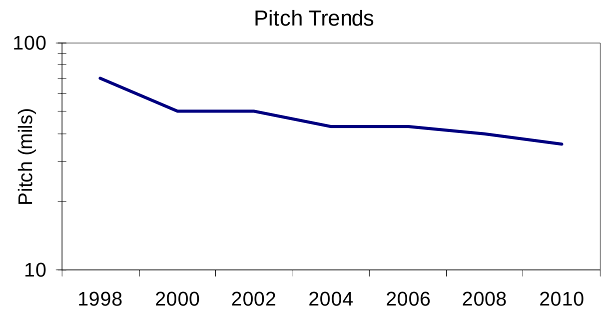


Figure 15: Pitch trends

The solution space requires package and socket technologies that are pitch and pin-count scalable. The LGA package and socket provide a scalable solution to address these near-term requirements, although significant integration is required between these components and the motherboard to achieve success.

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REFERENCES

[1] Baldwin, C., Chickamenahalli, S., DeFord, B., Parmar, P., and Stone, B., "Next-Generation Package and Socket Considerations," *Intel Assembly & Test Technology Journal*, vol. 5, 2002, pp. 83-94.

[2] Chickamenahalli, S., Kang, J., Do, H., Radhakrishnan, K., Augustine, A., and Bhattacharya, A., "Socket Imax Analysis Methodology Applications," *Intel Assembly & Test Technology Journal*, vol. 6, 2003, pp. 65-72.

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